414 Rec'd PCT/PTO 1 4 NOV 2000

FORM PTO-1390 (Modified) (REV 11-98) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE

TRANSMITTAL LETTER TO THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US) CONCERNING A FILING UNDER 35 U.S.C. 371

ATTORNEY'S DOCKET NUMBER: RCA .89038

U.S. APPLICATION NO. (IF KNOWN, SEE 37 CFR): 09/700359

INTERNATIONAL APPLICATION NO.	INTERNATIONAL FILING DATE	PRIORITY DATE CLAIMED
PCT/US99/10227	11May1999 (11.05.99)	16May1998 (16.05.98)

TITLE OF INVENTION: A BUS ARRANGEMENT FOR A DRIVER OF A MATRIX DISPLAY

APPLICANT(S) FOR DO/EO/US: Roger Green Stewart and Frank Paul Cuomo

Applicant herewith submits to the United States Designated/Elected Office (DO/EO/US) the following items and other information:

1. ☒ This is a **FIRST** submission of items concerning a filing under 35 U.S.C. 371.
2. ☐ This is a **SECOND** or **SUBSEQUENT** submission of items concerning a filing under 35 U.S.C. 371.
3. ☒ This is an express request to begin national examination procedures (35 U.S.C. 371(f)) at any time rather than delay examination until the expiration of the applicable time limit set in 35 U.S.C. 371(b) and PCT Articles 22 and 39(1).
4. ☒ A proper Demand for International Preliminary Examination was made by the 19th month from the earliest claimed priority date.
5. ☒ A copy of the International Application as filed (35 U.S.C. 371 (c) (2))
   a. ☐ is transmitted herewith (required only if not transmitted by the International Bureau).
   b. ☒ has been transmitted by the International Bureau.
   c. ☐ is not required, as the application was filed in the United States Receiving Office (RO/US).
6. ☐ A translation of the International Application into English (35 U.S.C. 371(c)(2)).
7. ☒ A copy of the International Search Report (PCT/ISA/210). attached to Item 13
8. ☒ Amendments to the claims of the International Application under PCT Article 19 (35 U.S.C. 371 (c)(3))
   a. ☐ are transmitted herewith (required only if not transmitted by the International Bureau).
   b. ☐ have been transmitted by the International Bureau.
   c. ☐ have not been made; however, the time limit for making such amendments has NOT expired.
   d. ☒ have not been made and will not be made.
9. ☐ A translation of the amendments to the claims under PCT Article 19 (35 U.S.C. 371(c)(3)).
10. ☒ An oath or declaration of the inventor(s) (35 U.S.C. 371 (c)(4)).
11. ☒ A copy of the International Preliminary Examination Report (PCT/IPEA/409).
12. ☐ A translation of the annexes to the International Preliminary Examination Report under PCT Article 36 (35 U.S.C. 371 (c)(5)).

Items 13 to 20 below concern document(s) or information included:

13. ☒ An Information Disclosure Statement under 37 CFR 1.97 and 1.98. with references attached
14. ☒ An assignment document for recording. A separate cover sheet in compliance with 37 CFR 3.28 and 3.31 is included.
15. ☒ A **FIRST** preliminary amendment.
16. ☐ A **SECOND** or **SUBSEQUENT** preliminary amendment.
17. ☐ A substitute specification.
18. ☐ A change of power of attorney and/or address letter.
19. ☒ Certificate of Mailing by Express Mail 20. Return postcard receipt
20. ☒ Other items or information: **CERTIFICATE OF MAILING UNDER 37 CFR 1.10**

EL667108425US — "Express Mail" mailing no.

14 November 2000 — Date of Deposit

I hereby certify that this application is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 CFR 1.10 on the date indicated above and is addressed to the Assistant Commissioner for Patents, Washington, D.C. 20231.

DAVIDA FORNAROTTO — Typed or printed name of person mailing application

Davida Fornarotto — Signature of person mailing application

PCTUS1/REV03

U.S. APPLICATION NO. (IF KNOWN, SEE 37 CFR)	INTERNATIONAL APPLICATION NO.	ATTORNEY'S DOCKET NUMBER
09/700359	PCT/US99/10227	RCA 89038

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21. The following fees are submitted:.	CALCULATIONS	PTO USE ONLY
BASIC NATIONAL FEE (37 CFR 1.492 (a) (1) - (5)) :		
☐ Neither international preliminary examination fee (37 CFR 1.482) nor international search fee (37 CFR 1.445(a)(2) paid to USPTO and International Search Report not prepared by the EPO or JPO $1000.00		
☒ International preliminary examination fee (37 CFR 1.482) not paid to USPTO but Internation Search Report prepared by the EPO or JPO $860.00		
☐ International preliminary examination fee (37 CFR 1.482) not paid to USPTO but international search fee (37 CFR 1.445(a)(2)) paid to USPTO $710.00		
☐ International preliminary examination fee paid to USPTO (37 CFR 1.482) but all claims did not satisfy provisions of PCT Article 33(1)-(4) $690.00		
☐ International preliminary examination fee paid to USPTO (37 CFR 1.482) and all claims satisfied provisions of PCT Article 33(1)-(4) $100.00		
ENTER APPROPRIATE BASIC FEE AMOUNT =	860.00	
Surcharge of **$130.00** for furnishing the oath or declaration later than ☐ 20 ☐ 30 months from the earliest claimed priority date (37 CFR 1.492 (e)).		

CLAIMS	NUMBER FILED	NUMBER EXTRA	RATE		
Total claims	9 - 20 =	0	x $18.00		
Independent claims	3 - 3 =	0	x $80.00		
Multiple Dependent Claims **(check if applicable).**			☐		
TOTAL OF ABOVE CALCULATIONS			=	860.00	
Reduction of 1/2 for filing by small entity, if applicable. Verified Small Entity Statement must also be filed (Note 37 CFR 1.9, 1.27, 1.28) **(check if applicable).**			☐		
SUBTOTAL			=	860.00	
Processing fee of **$130.00** for furnishing the English translation later than ☐ 20 ☐ 30 months from the earliest claimed priority date (37 CFR 1.492 (f)).			+		
TOTAL NATIONAL FEE			=	860.00	
Fee for recording the enclosed assignment (37 CFR 1.21(h)). The assignment must be accompanied by an appropriate cover sheet (37 CFR 3.28, 3.31) **(check if applicable).**			☐	40.00	
TOTAL FEES ENCLOSED			=	900.00	
			Amount to be: refunded		$
			charged		$ 900.00

☐ A check in the amount of to cover the above fees is enclosed.

☒ Please charge my Deposit Account No. 07-0832 in the amount of $900.00 to cover the above fees.
A duplicate copy of this sheet is enclosed.

☒ The Commissioner is hereby authorized to charge any fees which may be required, or credit any overpayment to Deposit Account No. 07-0832 A duplicate copy of this sheet is enclosed.

NOTE: Where an appropriate time limit under 37 CFR 1.494 or 1.495 has not been met, a petition to revive (37 CFR 1.137(a) or (b)) must be filed and granted to restore the application to pending status.

SEND ALL CORRESPONDENCE TO:

Mr. Joseph S. Tripoli
THOMSON multimedia Licensing Inc.
Patent Department
PO Box 5312
Princeton, New Jersey 08540

RECEIVED
NOV 15 2000
PCT LEGAL ADMINISTRATION

SIGNATURE

Sammy S. Henig
NAME

30,263
REGISTRATION NUMBER

November 14, 2000
DATE

EXPRESS MAIL LABEL NO. EL667106425US

RCA 89938 09/700359
529 Rec'd PCT/PTO 14 NOV 2000

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant	:	ROGER GREEN STEWART and FRANK PAUL CUOMO
Filed	:	Herewith
For	:	A BUS ARRANGEMENT FOR A DRIVER OF A MATRIX DISPLAY

PRELIMINARY AMENDMENT

Hon. Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

In the US national phase application of PCT/US99/10227 filed herewith, please enter the following amendments.

IN THE TITLE:

Please amend the title of the application to read "A BUS ARRANGEMENT FOR A DRIVER OF A MATRIX DISPLAY".

IN THE DESCRIPTION:

Page 1, line 1, delete "A BUSS ARRANGEMENT FOR A DISPLAY DRIVER" and insert -- A BUS ARRANGEMENT FOR A DRIVER OF A MATRIX DISPLAY--.

IN THE ABSTRACT:

Please add the Abstract as follows.

-- A demultiplexer applies picture information to pixels arranged in an array of a display device having columns and rows. The demultiplexer includes transistor switches each having a control terminal, an input terminal and an output terminal. A first bus couples switch control signals to the control terminals of the switches. The conductors of a first bus extend in a region containing each of the switches to form a global bus arrangement. Local buses have each conductors coupled to the input terminals of the switches associated with the individual local bus. The output terminals of the switches associated with the individual local bus are coupled to corresponding, consecutively disposed column conductors of the array. The individual local bus has a section that crosses over the first bus and a second section extending between the crossover section and the input terminals of

the associated switches. The conductors of the second section extend in a region containing the associated switches and are absent from regions containing switches associated with the other local buses to obtain bus separation forming a local clustering bus arrangement. --

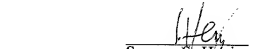
REMARKS

The above amendments to the Title and the Description have been made to incorporate the amendment of the title, which occurred during the prosecution of the PCT application.

To meet the requirements of the United States, the Abstract (as amended during the prosecution of the PCT application) is added.

No fee is believed to have been incurred by virtue of this amendment. However if a fee is incurred on the basis of this amendment, please charge such fee against deposit account 07-0832

Respectfully submitted,
ROGER GREEN STEWART
FRANK PAUL CUOMO



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609/734-9751

THOMSON multimedia Licensing Inc.
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PO Box 5312
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November 14, 2000

09/700359
PTO/PCT Rec'd 14 NOV 2000

A BUSS ARRANGEMENT FOR A DISPLAY DRIVER

This invention relates generally to a buss arrangement for display devices and particularly to a system for applying brightness signals to pixels of a display device, such as a liquid crystal display (LCD) or a plasma display.

Display devices, such as liquid crystal displays or plasma displays, are composed of a matrix or an array of pixels arranged horizontally in rows and vertically in columns. The video information to be displayed is applied as brightness (gray scale) signals to data lines which are individually associated with each column of pixels. The rows of pixels are sequentially scanned and the capacitances of the pixels within the activated row are charged to the various brightness levels in accordance with the levels of the brightness signals applied to the individual columns.

Brightness information to be applied to the array of pixels may be formatted into M brightness information signals developed in M parallel brightness information carrying conductors, for example, M=100. The M brightness information signals are applied to an input port of an input demultiplexer of the array. During each horizontal line interval of the video signal, the demultiplexer converts the M brightness information signals to MXN signals developed in MXN parallel conductors that are coupled via MXN data line drives to MXN column conductors of the array. The input demultiplexer may be formed by MXN thin film transistor (TFT's). Groups of M parallel conductors are successively selected, during each horizontal line interval of the video signal. The selection of each group of M parallel conductors is obtained by selection pulse signals developed in a bus of N parallel conductors.

The capacitance of the input bussing structure associated with the N selection parallel conductors and the input bussing

structure associated with the M brightness information carrying parallel conductors can be a major source of both power dissipation and yield loss, especially for higher resolution self-scanned Active-Matrix Liquid Crystal Displays (AMLCDs). Long metal runs across the display and multiple crossovers (Source/Drain metal-to-Gate metal) cause significant capacitive loads, resulting in both capacitance shorting failures, unwanted crosstalk among the brightness information carrying conductors and excessive dynamic power dissipation. It is desirable to reduce the number of crossovers of the input bussing structure associated with the N selection parallel conductors and of the input bussing structure associated with the M brightness information carrying parallel conductors.

An arrangement, embodying an inventive feature, for transferring pixel information with respect to pixels arranged in columns and rows of an array of a display device includes semiconductor switches. Each switch has a first terminal, a second terminal and a third terminal. A first buss is coupled to a first plurality of terminals for communicating signals between the first plurality of terminals and the first terminals of the switches. Local busses that are separated from one another are provided. A given local buss has a first buss section coupled to a second plurality of terminals associated with the given local buss and extends in a manner to cross over the first buss. The local buss has a second buss section extending from the first buss section has conductors coupled in a local, clustering buss arrangement to the second terminals of switches associated with the given local buss. The associated switches have their third terminals coupled to consecutively disposed column conductors, respectively, of the array.

FIGURE 1 illustrates an AMLCD with integrated driver circuits, according to an aspect of the invention, when incorporating the bussing arrangement of FIGURE 3;

FIGURE 2 illustrates a prior art bussing structure; and

FIGURE 3 illustrates a bussing structure, in accordance with an aspect of the invention, that may be incorporated in the arrangement of FIGURE 1.

FIGURE 1 illustrates an integrated driver arrangement for storing information in an SVGA liquid crystal array. It should be understood that the invention may be utilized for storing information in pixels of a plasma display. Analog circuitry 11 receives a video signal representative of picture information to be displayed from, for example, an antenna 12. The analog circuitry 11 provides a video signal on a line 13 as an input signal to an analog-to-digital converter (A/D) 14.

The television signal from the analog circuitry 11 is to be displayed on a liquid crystal array 16 which is composed of a large number of pixel elements, such as a liquid crystal cell 16a, arranged horizontally in m = 600 rows and vertically in n = 2400 columns. Liquid crystal array 16 includes n = 2400 columns of data lines 17, one for each of the vertical columns of liquid crystal cells 16a, and m = 600 select lines 18, one for each of the horizontal rows of liquid crystal cells 16a.

A/D converter 14 includes an output bus 19 to provide brightness levels, or gray scale codes, to a memory 21 having 100 groups of output lines 22. Each group of output lines 22 of memory 21 applies the stored digital information to a corresponding digital-to-analog (D/A) converter 23. There are 100 D/A converters 23 that correspond to the 100 groups of lines 22, respectively. An output analog signal DBS(j) from a given D/A converter 23 is coupled via a

corresponding brightness information carrying conductor DB(j) to a demultiplexer transistor MN1 associated with a corresponding column. Transistors MN1 may be thin film transistors (TFTs). The symbol (j) assumes values from 1 to 100 associated with the 100 D/A converter 23. Demultiplexer transistor MN1 applies the information of signal DBS(j) developed on corresponding brightness information carrying conductor DB(j) to a corresponding sampling capacitor C43 for storing an analog signal VC43 in capacitor C43. Signal VC43 is coupled to a corresponding data line driver 100 that drives corresponding data line 17 associated with a corresponding column.

A select line scanner 60 produces row select signals in lines 18 for selecting, in a conventional manner, a given row of array 16. The voltages developed in 100 data lines 17 are applied during a 32 microsecond line time to pixels 16a of the selected row.

The sampling in a given group of 100 signals DBS(j) of FIGURE 1 developed in brightness information carrying conductors DB(j) occurs simultaneously under the control of a corresponding data-word pulse signal DWS(i) forming a selection word. There are 24 pulse signals DWS(i), developed on 24 separate data-word conductors DW(i), that occur successively during a 32 microsecond horizontal line time. The symbol (i) assumes values from 1 to 24 associated with the 24 separate conductors DW(i). Each pulse signal DWS(i) controls the sampling of a corresponding group of 100 signals DBS(j) in capacitors C43.

To provide an efficient time utilization, a two-stage pipeline cycle may be used. Signals DBS(j) are demultiplexed and stored in 2400 capacitors C43 by the operation of pulse signals DWS(i). Then, the information in capacitors C43 is transferred simultaneously to data line driver 100. Thus, capacitors C43 become

available for the demultiplexing of the next row information, while the previous row information is applied to the pixels.

Except for the bussing arrangement, as described later on, the circuitry of FIGURE 1 may operate, for example, similarly to that described in, for example, U.S. Patent No. 5,673,063 in the name of Sherman Weisbrod, entitled " A DATA LINE DRIVER FOR APPLYING BRIGHTNESS SIGNALS TO A DISPLAY ". A possible bussing arrangement of conductors DW(i) and DB(j) is explained in connection with FIGURE 2. The bussing arrangement of conductors DW(i) and DB(j), embodying an inventive feature, is explained in connection with FIGURE 3. Similar symbols and numerals in FIGURES 1, 2 and 3 indicate similar items or functions.

As explained before, the crossover capacitance of the input bussing structure associated with conductors DW(i) and DB(j) can be a major source of both power dissipation and yield loss, especially for higher resolution self-scanned Active Matrix Liquid Crystal Displays (AMLCDs). Long metal runs across the display and multiple crossovers (Source/Drain metal-to-Gate metal) cause significant capacitive loads, resulting in both capacitance shorting failures, unwanted crosstalk among the brightness information carrying conductors, and excessive dynamic power dissipation. The bussing arrangement of FIGURE 3 reduces the number of capacitive crossovers associated with the input buss structure thus reducing the power dissipation and improving yield.

In the bussing arrangement of FIGURE 2, all conductors DW(i), that develop gate signals DWS(i) of demultiplexer transistor MN1 of FIGURE 1, are bussed together or globally across the entire display. Each column of the array is associated with a corresponding transistor MN1 having a gate electrode connected to one of those buss conductors DW(i) via a corresponding extention conductor DWC(i).

Connection of extention conductor DWC(i) to the corresponding buss conductor DW(i), located closest to data scanner transistors MN1, does not cause excessive capacitance problem. However, making connection of a given extention conductor DWC(i) to the corresponding buss conductor DW(i) that is furthest away from data scanner transistors MN1 means that extension conductor DWC(i) must cross all of the other buss conductors DW(i) to which it is not connected. Capacitive coupling CP to the other conductors DW(i), is incurred at each cross over as shown in FIGURE 2.

Disadvantageously, the number of capacitive crossovers increases geometrically with the number of data-word conductors DW(i) according to the equation: number of crossovers = number of brightness information carrying conductors DB(j) x 1/2 x (number of data-word conductors DW(i)). It may be desirable to reduce the number of times conductors DWC(i) cross the buss of conductors DW(i) so as to reduce dynamic power dissipation and improve yield.

As shown in FIGURE 3, in a "cluster bussing" buss structure, embodying an inventive feature, the brightness information carrying conductors DB(j), instead of being arranged individually and uniformly across the display, are grouped together into local "clusters" such as, for example, brightness information carrying conductors DB(1)-DB(4). The cluster of brightness information carrying conductors DB(1)-DB(4) are coupled to four transistors MN1 having gate electrodes that share, in common, conductor DW(24). In this example, the number of crossovers of brightness information carrying conductors DB(j)-to-data-word conductors DW(i) have been reduced by a factor of about 4:1. This, advantageously, reduces dynamic power dissipation, improves yield and reduces the crosstalk among the brightness information carrying-conductors.

In the arrangement of FIGURE 2, transistors MN1 associated with 24 adjacent columns of matrix 16 of FIGURE 1 have gates that are controlled by consecutive data-word signals DWS(i) and apply a common signal DBS(i) to the corresponding columns. In comparison, in the arrangement of FIGURE 3, transistors MN1 associated with 4 adjacent columns of matrix 16 of FIGURE 1 have gates that are controlled by common data-word signal DW(24) and apply 4 different signals DBS(i) to the corresponding columns.

The cluster bussing arrangement adds a multiplicity of new local sub-arrays DBSA to the bus structure. Although these new local sub-arrays do add some additional crossovers of their own (2.5 per brightness information carrying conductor), this is a small price to pay for reducing the average number of crossovers in the main brightness information carrying conductor to data-word conductor matrix from 20/data-line to only 5/data-line. The total capacitive coupling in the input buss structure is thereby cut by a factor of approximately 4 using the cluster buss technique. For example: in a display with 100 DB(j) and 24 DW(i) the total number of crossovers is 28,800 using the buss technique of FIGURE 2, while cluster bussing of FIGURE 3 yields 7450 total crossovers.

The primary advantages of cluster bussing, therefore, include higher yield, lower power dissipation, and reduced crosstalk. However, another advantage to cluster bussing is that we now break up the pattern of consecutive columns connected to a single signal DBS(j). Small errors in signal DBS(j)-to-signal DBS(j) will normally result in noticeable "block" errors because the human eye is very sensitive to large block patterns. Using the cluster buss technique, the blocks are broken-up into a finer pitch that is, advantageously, less obvious to the viewer.

Thus, whenever demultiplexing is done with a matrix of 2 signal types involving typically 20 or more lines, the structure may be improved through the addition of clusters of sub-arrays to reduce the complexity and capacitance of the main array.

WHAT IS CLAIMED IS:

1. An arrangement for transferring pixel information with respect to pixels arranged in columns and rows of an array of a display device, comprising:

a plurality of semiconductor switches, each having a first terminal, a second terminal and a third terminal;

a first buss coupled to a first plurality of terminals for communicating corresponding signals; and

a plurality of local busses that are separated from one another for communicating corresponding signals, a given local buss having a first buss section coupled to a second plurality of terminals associated with said given local buss and extending in a manner to cross over said first buss and a second buss section extending from said first buss section and having conductors thereof coupled in a local, clustering buss arrangement to the second terminals of switches associated with said given local buss of said plurality of switches, the associated switches having the third terminals thereof coupled to consecutively disposed column conductors, respectively, of said array.

2. An arrangement according to Claim 1 wherein said first plurality of terminals, develop switch control signals and said second plurality of terminals develop picture information signals for said switches to form a demultiplexer for storing the picture information in said pixels of said array.

3. An arrangement according to Claim 1 wherein said associated switches including a plurality of sub-groups of switches. the switches of a given sub-group having the first terminals thereof coupled in common to a corresponding conductor of said first buss and the third terminals thereof being coupled to consecutively disposed column conductors, respectively, of said array.

4. An arrangement according to Claim 1 wherein the conductors of said second buss section of said given local buss are disposed in a vicinity of said switches associated with said given buss and remotely from switches associated with the other local busses of said plurality of local busses to provide buss separation for obtaining the local clustering buss arrangement.

5. An arrangement according to Claim 1 wherein the conductors of said first buss extend along each of said plurality of semiconductor switches to form a global buss arrangement.

6. An arrangement according to Claim 1 wherein said third terminal of each of said semiconductor switches is coupled to an input terminal of a corresponding data line driver.

7. A signal demultiplexer for a display panel, comprising:

a plurality of clusters of switches, each cluster having ordinally numbered switches 1 thru n arranged sequentially, and each switch having respective input, output and control terminals with the control terminals of all switches in each cluster connected to

a common control terminal, and having respective output terminals coupled to successive data lines on said display panel;

a plurality of clusters of data busses, each cluster of data busses having ordinally numbered conductors 1 thru n, the ordinally numbered conductors of respective clusters of data busses being coupled to input terminals of corresponding ordinally numbered switches of a plurality of said clusters of switches;

a control buss including a plurality of conductors, said control buss arranged to crossover said plurality of clusters of data busses; and

connections between ones of said plurality of conductors of said control buss and respective common control terminals of said clusters of switches.

8. A signal demultiplexer for a display panel, comprising:

a plurality of clusters of switches, a given cluster having ordinally numbered switches arranged sequentially, and each switch having respective input, output and control terminals, the output terminals coupled to successive data lines on said display panel;

a cluster of data busses, a given data bus thereof having ordinally numbered conductors arranged sequentially, a given conductor of said given data buss being coupled in common to the input terminal of each switch having the same ordinal number that corresponds to the ordinal number of said given conductor and being included in each cluster of said switches that is associated with said given data bus;

a control buss including a plurality of conductors, said control buss arranged to crossover said clusters of data busses; and

connections between ones of said plurality of conductors of said control buss and respective control terminals of said clusters of switches.

9. A signal demultiplexer according to Claim 8 wherein the control terminals of all the switches in each cluster of switches are connected in common to a corresponding conductor of said control buss.

SUBSTITUTE SHEET (RULE 26)

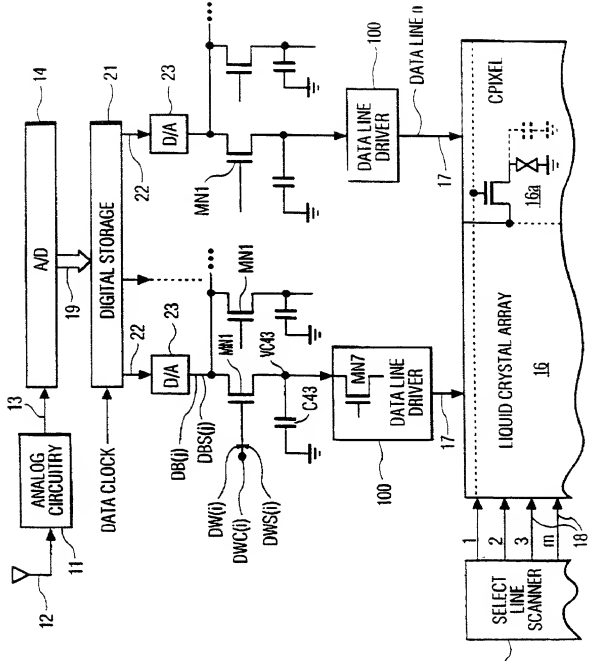
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FIG. 1

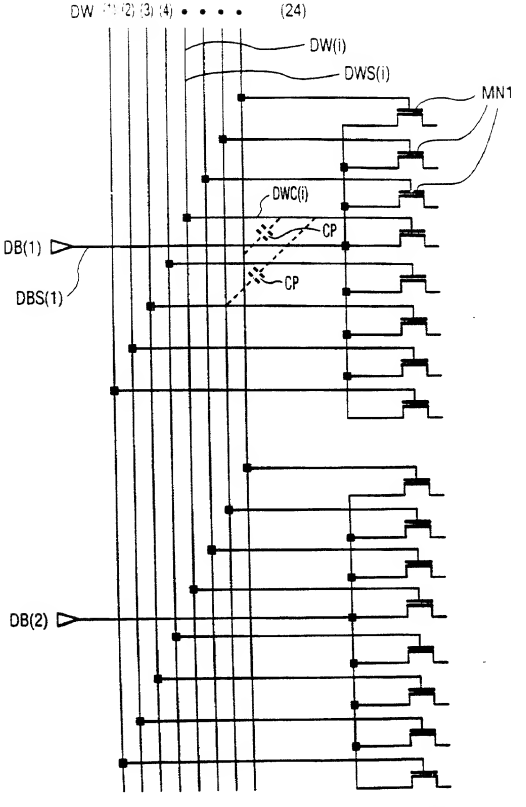

FIG. 2 PRIOR ART

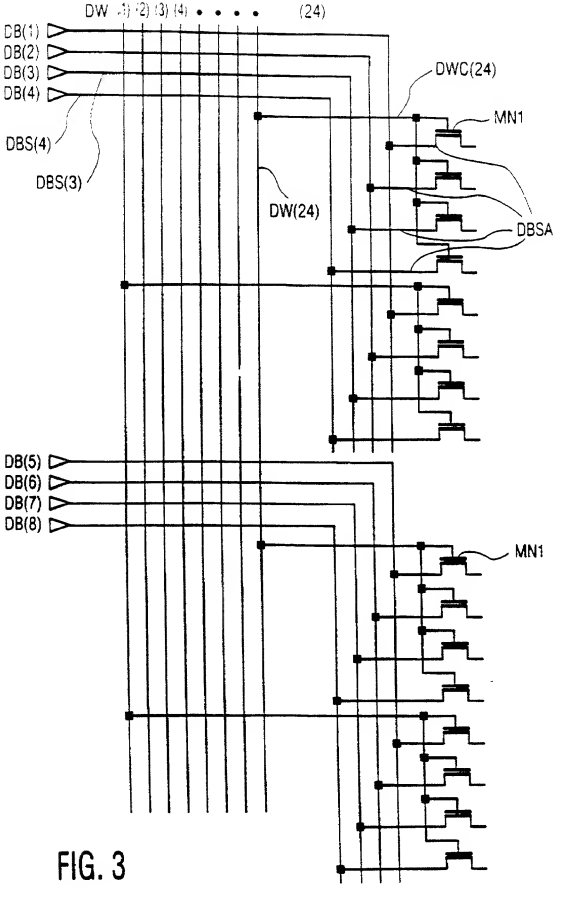
DW (1) (2) (3) (4) • • • • (24)
DB(1)
DB(2)
DB(3)
DB(4)
DBS(4)
DBS(3)
DWC(24)
MN1
DW(24)
DBSA
DB(5)
DB(6)
DB(7)
DB(8)
MN1

FIG. 3

Please type a plus sign (+) inside this box → [+]

PTO/SB/01 (12-97)
Approved for use through 9/30/00. OMB 0651-0032
Patent and Trademark Office, U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

DECLARATION FOR UTILITY OR DESIGN PATENT APPLICATION (37 CFR 1.63)

☐ Declaration Submitted with Initial Filing OR ☒ Declaration Submitted after Initial Filing (surcharge (37 CFR 1.16 (e)) required)

Attorney Docket Number	RCA 89038
First Named Inventor	Roger Green Stewart et al
COMPLETE IF KNOWN	
Application Number	
Filing Date	
Group Art Unit	
Examiner Name	

As a below named inventor, I hereby declare

My residence, post office address, and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

A BUS ARRANGEMENT FOR A DRIVER OF A MATRIX DISPLAY

(Title of the Invention)

the specification of which
☐ is attached hereto
OR
☒ was filed on (MM/DD/YYYY) May 11, 1999 as United States Application Number or PCT International Application Number PCT/US99/10227 and was amended on (MM/DD/YYYY) _____ (if applicable).

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment specifically referred to above.

I acknowledge the duty to disclose information which is material to patentability as defined in 37 CFR 1.56

I hereby claim foreign priority benefits under 35 U.S.C. 119(a)-(d) or 365(b) of any foreign application(s) for patent or inventor's certificate, or 365(a) of any PCT international application which designated at least one country other than the United States of America, listed below and have also identified below, by checking the box, any foreign application for patent or inventor's certificate, or of any PCT international application having a filing date before that of the application on which priority is claimed.

Prior Foreign Application Number(s)	Country	Foreign Filing Date (MM/DD/YYYY)	Priority Not Claimed	Certified Copy Attached? YES	NO
			☐	☐	☐
			☐	☐	☐
			☐	☐	☐
			☐	☐	☐

☐ Additional foreign application numbers are listed on a supplemental priority data sheet PTO/SB/02B attached hereto.

I hereby claim the benefit under 35 U.S.C. 119(e) of any United States provisional application(s) listed below

Application Number(s)	Filing Date (MM/DD/YYYY)	
60/085,766	May 16, 1998	☐ Additional provisional application numbers are listed on a supplemental priority data sheet PTO/SB/02B attached hereto.

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DECLARATION — Utility or Design Patent Application

I hereby claim the benefit under 35 U.S.C. 120 of any United States application(s), or 365(c) of any PCT international application designating the United States of America, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International application in the manner provided by the first paragraph of 35 U.S.C. 112, I acknowledge the duty to disclose information which is material to patentability as defined in 37 CFR 1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application.

U.S. Parent Application or PCT Parent Number	Parent Filing Date (MM/DD/YYYY)	Parent Patent Number (if applicable)
PCT/US99/10227	May 11, 1999	

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As a named inventor, I hereby appoint the following registered practitioner(s) to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith:

☐ Customer Number
OR
☒ Registered practitioner(s) name/registration number listed below

Place Customer Number Bar Code Label here

Name	Registration Number	Name	Registration Number
JOSEPH S. TRIPOLI	26,040		
JOSEPH J. LAKS	27,914 (3)		
SAMMY S. HENIG	30,263		

☐ Additional registered practitioner(s) named on supplemental Registered Practitioner Information sheet PTO/SB/02C attached hereto

Direct all correspondence to: ☐ Customer Number or Bar Code Label [ ] OR ☒ Correspondence address below

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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true, and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under 18 U.S.C. 1001 and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Name of Sole or First Inventor: ☐ A petition has been filed for this unsigned inventor

Given Name (first and middle [if any])	Family Name or Surname
ROGER GREEN	STEWART

Inventor's Signature	Roger Green Stewart					Date	11/10/00
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☒ Additional inventors are being named on the 1 supplemental Additional Inventor(s) sheet(s) PTO/SB/02A attached hereto

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DECLARATION

ADDITIONAL INVENTOR(S)
Supplemental Sheet
Page 1 of 1

Name of Additional Joint Inventor, if any:		☐ A petition has been filed for this unsigned inventor					
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Residence: City		State		Country		Citizenship	
Post Office Address							
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City		State		ZIP		Country	

Name of Additional Joint Inventor, if any:		☐ A petition has been filed for this unsigned inventor					
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Inventor's Signature						Date	
Residence: City		State		Country		Citizenship	
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